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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/768,246	01/25/2001	Kazushi Higashi	2001_0055	3700	
513	7590 10/04/2002				
	OTH, LIND & PONAC	EXAMINER			
2033 K STREET N. W. SUITE 800			PAREKH, NITIN		
WASHING	ΓON, DC 20006-1021		ART UNIT	PAPER NUMBER	
			2811		
			DATE MAILED: 10/04/2002		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No).	Applicant(s)	11 /
•	A ation Cumman	09/768,246	\cup	HIGASHI ET AL.	p
Offic	e Action Summary	Examiner		Art Unit	
		Nitin Parekh		2811	_
The MA Period for Reply	ILING DATE of this communication app	ears on the cov	er sheet with the c	correspondence addr	ess
THE MAILING - Extensions of time after SIX (6) MON - If the period for re, - If NO period for re Failure to reply with - Any reply received	D STATUTORY PERIOD FOR REPLY DATE OF THIS COMMUNICATION. It may be available under the provisions of 37 CFR 1.13 THS from the mailing date of this communication. Doly specified above is less than thirty (30) days, a reply ply is specified above, the maximum statutory period whin the set or extended period for reply will, by statute, by the Office later than three months after the mailing in adjustment. See 37 CFR 1.704(b).	36(a). In no event, how within the statutory modern and will expir cause the application	wever, may a reply be tin inimum of thirty (30) day e SIX (6) MONTHS from to become ABANDONE	nely filed s will be considered timely. the mailing date of this comr D (35 U.S.C. & 133)	nunication.
1)☐ Respon	sive to communication(s) filed on <u>08 J</u>	uly 2002 .			
2a)☐ This act	tion is FINAL . 2b)⊠ Thi	is action is non-	final.		
3) Since the closed in Disposition of Cla	nis application is in condition for allowant n accordance with the practice under a nims	nce except for Ex parte Quayle	formal matters, pr e, 1935 C.D. 11, 4	rosecution as to the 153 O.G. 213.	merits is
4)⊠ Claim(s)	1-20 is/are pending in the application				
4a) Of the	e above claim(s) <u>1-3,6,10 and 13-20</u> is	/are withdrawn	from consideration	on.	
5) Claim(s)	is/are allowed.				
6)⊠ Claim(s)	4,5,7-9,11 and 12 is/are rejected.				
7) Claim(s)	is/are objected to.				
8) Claim(s)	are subject to restriction and/or	election requir	ement.		
Application Paper	rs				
9)∏ The speci	fication is objected to by the Examiner	•.			
	ng(s) filed on is/are: a)☐ accep		•		
	it may not request that any objection to the	drawing(s) be h	eld in abeyance. Se	ee 37 CFR 1.85(a).	
	osed drawing correction filed on			oved by the Examiner.	
	ved, corrected drawings are required in rep		ction.		
	or declaration is objected to by the Exa	aminer.			
	U.S.C. §§ 119 and 120				
	edgment is made of a claim for foreign	priority under 3	35 U.S.C. § 119(a)-(d) or (f).	
a)∏ All b)[☐ Some * c)⊠ None of:				
1.⊠ Ce	rtified copies of the priority documents	s have been red	eived.		
2. Ce	rtified copies of the priority documents	s have been rec	eived in Applicati	on No	
	pies of the certified copies of the prior application from the International Bur tached detailed Office action for a list of	eau (PCT Rule	17.2(a)).		age
14) Acknowled	gment is made of a claim for domestic	priority under	35 U.S.C. § 119(e	e) (to a provisional a	oplication).
_a) 🔲 The t	ranslation of the foreign language prodgment is made of a claim for domesti	visional applica	tion has been rec	eived.	
Attachment(s)		, , , , , , , , , , , , , , , , , , , ,	33 . 20	· ····································	
3) Nformation Discle	ices Cited (PTO-892) erson's Patent Drawing Review (PTO-948) osure Statement(s) (PTO-1449) Paper No(s) <u>3 a</u>	4)	Interview Summary Notice of Informal F Other:	(PTO-413) Paper No(s). Patent Application (PTO-1	. 52)
S. Patent and Trademark Office PTO-326 (Rev. 04-01)	Office Ac	tion Summary		Part of Pa	per No. 11

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Election/Restrictions

1. Election of claims 4-12 directed to the Embodiment 3 is acknowledged.

However, claims 6 and 10 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 6 and 10 are directed to Embodiment 6 (Fig. 7-10; see paper # 8 and 5). Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits.

Accordingly, claims 6 and 10 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Double Patenting

2. NON-STATUTORY

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

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A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U.S. Patent No. 6207549.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant claim 4 is generic to the claims 1 and 2 of U.S. Patent No. 6207549, the generic features/elements comprising a semiconductor arrangement in which a bump electrode is bonded to a circuit forming surface of an integrated circuit (IC)/chip by a method, the method comprising operating a bonding capillary at a ball bond forming position to form a ball bond portion on the IC electrode, moving the capillary upward, sideways and downward with respect the IC electrode, bonding a wire to the ball bond portion, cutting the wire, the wire being prevented from coming in contact with portions around the ball bond other than the ball bond portion; wherein the bump electrode comprising a first protrusion portion formed by once melting and solidifying a wire and its periphery, being bonded to the IC electrode and

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further having a wire material portion in the vicinity of the melted portion being bonded and extended downwardly from the vertex portion, a second formed of an unmelted portion of the wire and being extended from the first protrusion, the bump electrode having the first and second protrusions being contacted or put close with the respective electrode when the IC chip is conventionally mounted on a circuit board.

The generic claims are generally considered obvious over more specific claims.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 7, line 2 cites: "...said formed portion has a <u>base portion bonded to said</u> electrode..."

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However, the description in specification and Figures (14B, 16, etc.) show the base portion of the bump electrode being bonded to the IC electrode and not to the said electrode on the circuit board.

Claim Rejections - 35 USC § 103

- 6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 4, 5, 7-9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Yasuzato et al (US Pat. 5060843), Khandros (US Pat. 5476211) and Khandros et al (US Pat. 5917707).

Regarding claim 4, the APA discloses a semiconductor arrangement in which a bump electrode is bonded to a circuit forming surface of an integrated circuit (IC)/chip by a method comprising:

- operating a bonding capillary at a ball bond forming position to form a ball bond portion on the IC electrode (106a and 104 respectively in Fig. 17A-C; Fig. 20A;
 Specification pages 1 and 2)
- moving the capillary upward with respect the IC electrode
- moving the capillary sideways and down ward with respect the IC electrode

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- bonding a wire to the ball bond portion, and
- cutting the wire, the wire being prevented from coming in contact with portions
 around the ball bond other than the ball bond portion itself by adjusting/presetting
 the descent position

(Fig. 17A-C; Fig. 20A; Specification pages 1 and 2).

wherein the bump electrode comprises:

- a first protrusion portion comprising a formed portion having a vertex/tip, (cone shaped bump portion in 106a), the formed portion formed by once melting and solidifying a wire and its periphery and is bonded to the IC electrode and further having a wire material portion (not numerically referenced in Fig. 20A-see the bonded wire portion connecting the second protrusion) in the vicinity of the melted portion being bonded and extended downwardly from the vertex portion
- a second protrusion (not numerically referenced in Fig. 20A- tail portion of the wire having a tip) formed of an unmelted portion of the wire and being extended from the first protrusion, and
- the bump electrode having the first and second protrusions are being contacted or put close with the respective electrode when the IC chip is conventionally mounted on a circuit board (Fig. 19A-C)

(Fig. 17A-20C; specification pages 1-3).

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The APA fails to specify the second protrusion being extended from the first protrusion beyond a planar area defined by projecting the first protrusion to a height approximately equal to that of the first protrusion with respect the IC electrode.

Khandros teaches using bump electrodes having a plurality of protrusions which extend beyond (33, 35, 63, etc. in Fig. 14-16; Col. 12 and 13) a planar area defined by projecting the first protrusion to a height approximately equal to that of the first protrusion with respect the IC electrode to achieve the flexibility for an interconnection.

Yasuzato et al teach using a bump electrode having a protrusion which extends beyond (23cc in Fig. 5A) a planar area defined by projecting the first protrusion to a height approximately equal to that of the first protrusion with respect the IC electrode.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second protrusion being extended from the first protrusion beyond a planar area defined by projecting the first protrusion to a height approximately equal to that of the first protrusion with respect the IC electrode so that the flexibility and capability for the interconnections can be improved using Khandros and Yasuzato et al's wiring structures in the APA.

Regarding claim 5, the claim elements have been addressed in the rejection as explained above for claim 4.

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Regarding claims 8 and 9, the APA further discloses the second protrusion (not numerically referenced in Fig. 20A- tail portion of the wire having a tip) being extended toward an outer end surface side of the semiconductor element without exceeding the outer end surface but fails to specify the same extending outwardly beyond the outer end surface of the semiconductor element.

Khandros et al teach using a variety of configurations where the bump protrusions extend outwardly beyond the outer end surface of the semiconductor element (Fig. 11, 12, etc.; Col. 9).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second protrusion being extended outwardly beyond the outer end surface of the semiconductor element so that the flexibility and capability for the interconnections can be improved using Khandros et al, Khandros and Yasuzato et al's wiring structures in the APA.

Regarding claim 11, the APA further discloses the ball bond portion and the wire having no circumscribed space (Fig. 20A).

Regarding claim 12, the claim elements have been addressed in the rejection as explained above for claim 4.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP

TOM THOMAS SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800

09-25-02